Design and Implementation of MAC Protocol based CDMA system for solving Near Far Effect using VHDL

Aakanksha Devrari, Adesh Kumar, Shraddha Singh, Amit Kumar

Abstract— The paper focuses on implementation of MAC protocol system for solving near far effect in Ad-hoc networks. The main issue in Direct Sequence Code Division Multiple access (DS-CDMA) Ad-hoc network is the issue of a near-far problem. The near-far problem can severely affect packet reception, and consequently, network throughput. In the article, focus is done on utilization of both power and medium access control approaches. For the problem, a design based on DS-CDMA system is developed and channel access is governed with the help of MAC protocol. Modelsim10.2 (MXE) tool is used for functional and logic verification of each block. The Xilinx Synthesis Technology (XST) of Xilinx ISE 14.2i tool is used for synthesis of transmitter and receiver using Virtex 5 FPGA.

Index Terms— Direct Sequence Spread Spectrum (DSSS), Medium Access Control (MAC) protocol, Gold Sequence Generator, Very High Speed Integrated Circuit Hardware Description Language (VHDL).

1 INTRODUCTION

The world's 1st cellular networks were introduced in the early 1980s, utilizing analog radio transmission technologies like Advanced mobile phone System (AMPS) [1]. CDMA networks were first launched in 1995, and it provided roughly ten times more capacity than analog networks. Since then, DS CDMA has become the earlier growing of all wireless technologies, with over a hundred million subscribers worldwide.

In [5] authors proposed the direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter and receiver is implemented in VHDL language for FPGA. In [7] author proposed the implementation of DS-CDMA transmitter using Verilog HDL. It explains the design for pseudo random Psuedo random Noise (PN) code and a direct sequence principle based wireless transmitter.

2. DIRECT SEQUENCE SPREAD SPECTRUM

Direct Sequence is the best known spread spectrum technique. The data signal is multiplied by a PN code. A PN code is a sequence of chips valued -1 and 1 (polar) or 0 and 1 (non-polar) and has a noise like properties,which results in low cross-correlation values among the codes and the difficulty to jam or detect a message. PN codes can be created by means of a linear feedback shift-register.

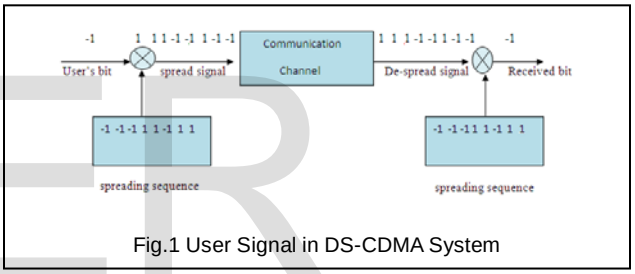
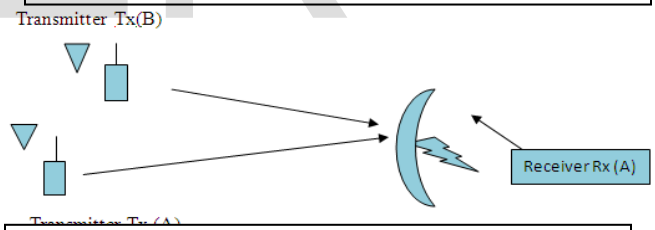
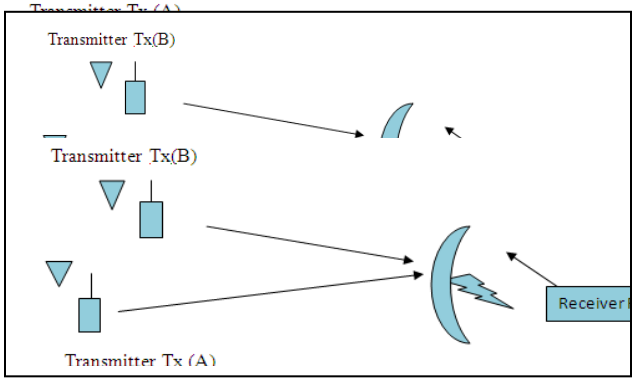


Fig.1 User Signal in DS-CDMA System





When all transmission powers are equal, and the receiver is much closer in distance to transmitter Tx(B) than Tx(A), the signal of Tx(B) will arrive at the receiver with a sufficiently larger power than that of the Tx(A), causing incorrect decoding of the transmission Tx(A).

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3 MAC PROTOCOL

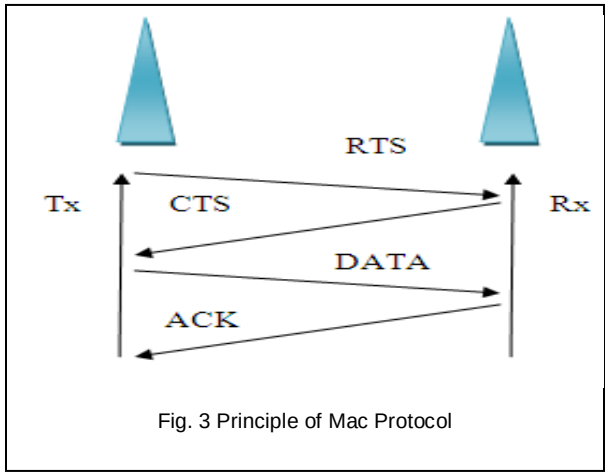

Fig. 3 Principle of Mac Protocol

In the RTS/CTS algorithm, the node which wants to send frames sends a request to send (RTS) frame to the destination node first, and after the destination node responds with a clear to send (CTS) frame immediately. Only when the source node receives the CTS transmitted from destination node accurately; the source node is allowed to transmit frames. Whenever the source node receives the CTS, it starts the transmission of data. In order to face the unreliability of the channel, the MAC protocol adds a positive acknowledgement (ACK) upon the reception of a data packet. The proposed MAC based DS-CDMA solution provides a methodology in which after receiving the MAC ID from the transmitters, receiver firstly checks for the destination MAC in the received signal. If the ID matches with the self ID of the receiver it will allow the transmitter to send the data further. This will always restrict the non intended transmitter to transmit the data to the non intended receiver by providing the transmitter the information to reduce its power for transmission if the MAC ID comparison match fails .Principle of MAC is shown in the figure.3.

3.1 Channel Access Mechanism

i) Step 1: If terminal 'j' has a packet to transmit, it sends a RTS packet at max. power value Pmax, and includes in this packet the maximum allowable power level (P(j)map) that terminal 'j' can use that will not disturb any ongoing reception in j's neighborhood. If the destination ID in RTS format matches with the self ID of receiver next step is to analyze power level.

- Request to Send (RTS) Frame: The frame structure for RTS signal is given below.

Destination address/ID	Transmitter address/ID	Duration	Data Size	Allowable power

Additional field

No. of bits in RTS Frame-
Destination address/ID = 2 bits
Transmitter address/ID = 2 bits
Data Size = n bits

ii) Step 2: The intended receiver 'i' receives the RTS packet, and uses the pre-determined Pmax value and the power of the received signal P(ji) received to estimate the channel gain .

$$G_{ji} = \frac{P^{ji}_{received}}{P_{max}} \qquad (1)$$

Terminal 'i' will be able to correctly decode the data packet if transmitted at a power P(ji)min given as-

$$P^{(ji)}_{min} = \mu^{*} (P_{thermal} + P_{MAI-current}{}^{(1)})/G_{ji} \qquad (2)$$

Where $P_{thermal}$ = Thermal noise power , $P_{MAI\ current}$ = Effective current MAI from all already ongoing (interfering) transmissions, G_{ji} = Channel Gain . All neighbors of terminal 'i' will have to defer their transmissions during terminal i's ongoing reception.

iii) Step 3: Calculate the Power that terminal 'j' is allowed to use to send to 'i' is given as-

$$P^{ji}_{allowed} = \xi_{max}\ \mu^{*}\ P_{thermal}\ /G_{ji} \qquad (3)$$

Where μ^{*} = Effective bit energy-to-noise spectral density ratio, Pthermal = Thermal noise power, ξ(max) = Maximum planned noise rise.

If P (ji)allowed < P(ji)min, 'i' responds with a negative CTS to inform 'j' that 'i' cannot proceed with j's transmission

If P (ji)allowed > P(ji)min , 'i' calculates the interference power tolerance PMAI -future(i) that it can endure from future unintended transmitters .

$$P_{MAI\ future}{}^{(i)} = 3W\ G_{ji}\ (P^{(ji)}_{allowed} - P^{(ji)}_{min})/\ 2\ \mu^{*} \qquad (4)$$

Where, W = Processing gain. 'i' equitably distributes this power tolerance among future potentially interfering users, μ^{*} = Effective bit energy-to-noise spectral density ratio.
When responding to j's RTS, terminal 'i' indicates in its CTS the power level $P^{(ji)}_{allowed}$ that 'j' must use. Also it inserts P (i) noise in the CTS packet and sends this packet back to terminal 'j' at maximum power.where, $P^{(i)}_{noise}$ = Interference tolerance that each future neighbor can add to terminal 'i'.

- Clear to Send (CTS) Frame : The frame structure for CTS signal is given below

Transmitter Address/ID	Destination Address/ID	Duration	Interference Tolerance Pi(noise)	Power Pji (allowed)

No. of bits in CTS Frame-
Destination address/ID = 2 bits
Transmitter address/ID = 2 bits

iv) Step 4 : Compute $P^{(s)}_{map}$; Potentially interfering terminal 's' hears the CTS message from 'i', then computes the channel gain Gsi between 's' and 'i' it also computes the maximum power $P^{(s)}_{map}$ that s can use in its future transmissions.

$$\mathbf{P^{(S)}_{map}} = \min (\mathbf{P^{(I)}_{noise}}/\mathbf{G_{si}}) \quad (5)$$

v) Step 5: 'j' sends data to 'i'. If transmission is successful, receiver 'i' responds 'j' with an ACK packet over the data channel using the same power level that would have been used if 'i' were to send a data packet to 'j'.

4 BLOCK DIAGRAM OF DS-CDMA MAC SYSTEM

Physical layer structure of MAC based DS-CDMA forward Link for Ad-hoc Network block diagram is shown in the Fig.4. The input data is represented by data which is a discrete N bit data. Convolution Encoder encodes redundant information into the transmitted signal, by improving the data capacity of the channel and making it immune to noise.

Next this encoded data stream acts as an input to Inter-leaver where shuffling (re-arrangement) of this data is done so as to remove burst errors in consecutive bits when data passes through channel.

In the next step Gold code sequence is generated using two pseudo noise sequences by means of a feedback shift register regulated by a timing clock. Decimator is used to reduce the data rate from 1.22Mbps to 19.2Kbps so as to make it compatible with the incoming data rate. Data bits then goes to DBPSK modulator.

Differential binary PSK is a non coherent form of phase shift keying which avoid the need for a coherent reference signal at the receiver. Walsh code is used which appears as arbitrary noise to a CDMA mobile terminal, unless that terminal makes the use of same code as the one which is used to encode the incoming signal. Next data goes to De inter leaver that rearranges the data in the proper sequence order.

In last step data bits is passed through Viterbi decoder that decodes de-interleaved data and results in the original sequence of data stream.

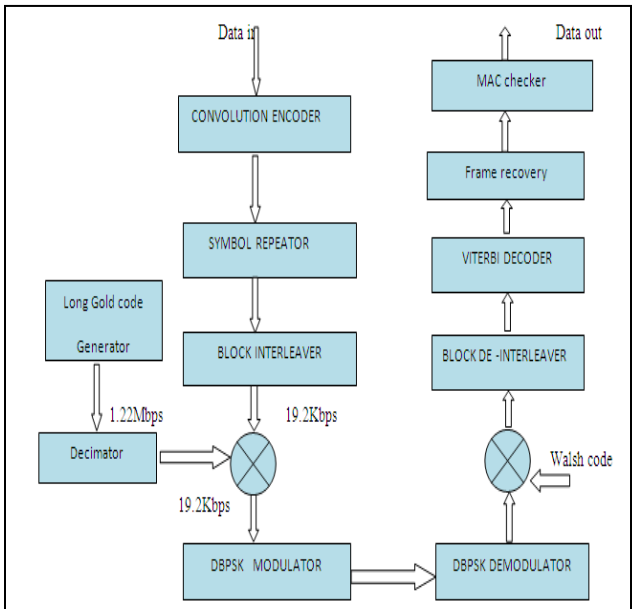

Fig.4 MAC based DS-CDMA link for Ad-hoc Network

5 SIMULATION RESULTS

The chip designing and synthesis is carried out in Xilinx 14.2 ISE software. The RTL view of the developed chip is shown in the figure 5 and the Modelsim simulation for the corresponding test vectors is shown in figure 6 and 7. Table 1 list the details supporting the RTL view and the Modelsim functionality. In the functional simulation, Reset is the input to reset, clk is used to provide a duty cycle and synchronize the transmitters and receivers. The transmitter and receivers are identified with their addresses, Tx_selection is an input address of transmitters and Rx_selection is an input address of receivers. Request to Send (RTS) is an input signal given the receiver to transmitter. Clear to Send (CTS) is the transmitter output to the receiver and ACK is the acknowledgment to the receiver from the transmitters. Data_stream is of 'N' bits and encoded_data_vector length is of 11 bits depends on the encoding scheme.

The convolution encoder is used to encode the data. The decoded_data_stream is of 'N' bits which are decoded using Viterbi algorithm and actual data transfer form transmitters and receivers, which is of 32 bits which is data_out [31:0]. The simulation is carried out with the assumption of four transmitter and four receivers. The transmitters have their addresses "00", "01", "10" and 11 sequentially. Similarly, receivers have their addresses "00", "01", "10" and 11 sequentially.

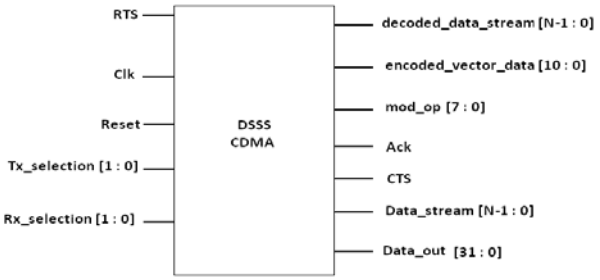

Fig.5 RTL view of DS-CDMA link for Ad-hoc Network

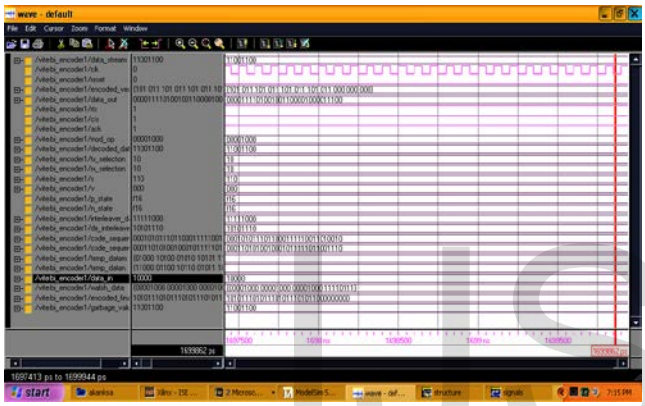

Fig.6 Simulation result for solving near far effect (MAC ID matches)

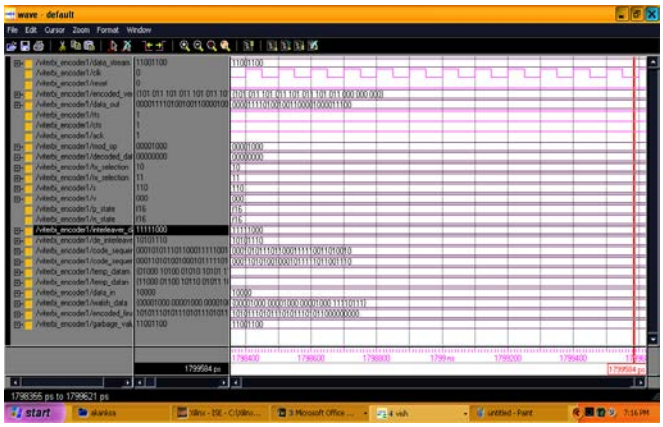

Fig.7 Simulation result for solving near far effect (MAC ID does not matches)

TABLE 1 DETAILS OF PIN

Pin	Description
Data_Stream	Input to the DS-CDMA MAC protocol (n bits)
Clk (1 bit)	Input to the DS-CDMA MAC used to provide positive (Rising edge) of clock system
Reset (1 bit)	Resets the data transmission states
Tx_selection (2 bits)	ID selection in RTS frame
Rx_selection (2 bits)	Self ID of receiver means receivers address
RTS	Request to Send signal from Transmitter to Receiver
CTS	Clear to Send signal from Receiver to Transmitter
ACK	Acknowledgement on data reception
Data_out	Output of gold code sequence generator
Mod_op	Modulated gold code sequence with interleaved data
Encoded_vector_data (32 bits)	Encoded vector of convolution encoder

TABLE 2 DEVICE UTILIZATION SUMMARY

Logic Utilization	Utilized	Available	Utilization
Number of slices	492	6144	8%
Number of slice flip flops	779	12288	6%
Number of 4 input LUTs	468	12288	3%
Number of bonded IOBs	97	240	40%
Number of GCLKs	3	32	9%

TABLE 3 TIMING PARAMETER SUMMARY

Speed Grade	-12

Minimum period	1.458ns
Minimum input arrival time before clock	3.073ns
Maximum output required time after clock	4.737ns
Maximum combinational path delay	5.868 ns
Total memory usage is	202240 KB
Add Generic Clock Buffer(BUFG)	32
Number of Regional Clock Buffers	16
Optimization goal	Speed
Optimization Effort	1
Slice Utilization Ratio	100

It is also clear that MAC protocol governs the complete data transfer from transmitter to receiver. Each transmitter and receiver is allotted a MAC ID and data is transmitted only if the allotted MAC ID of both Tx i.e (00,01,10,11) and Rx (00,01,10,11) matches this enables the data transfer from the intended transmitter to intended receiver only and restricts the non-intended transmitters and their data remains in a temporary state i.e a garbage value.

Transmitter firstly sends a RTS to receiver, Receiver detects the ID of the transmitter and if this ID matches with the self ID of receiver then it sends with positive CTS to transmitter. Transmitter on getting a CTS frame sends data and if this data reaches the destination i.e to the receiver correctly receiver sends an acknowledge signal (ACK) confirming the data reception. Reset is the sequential input when reset = 1, the output = 0 and when reset = 0, the clock pulse signal is synchronized to provide actual output.

CONCLUSION

In the paper a DS-CDMA MAC protocol system is designed and implemented on FPGA using VHDL language. From the simulation it is found that the hardware utilization in terms of no. of slices is 8%, no. of flip flops is 6 %, no. of bonded IOB's is 40%, no. of GCLKS is 9% and no. of 4 i/p LUTs is 3% which is extracted from the design. It is found that channel access mechanism approach adjusts the desired

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